Microwave PtSi–Si Schottky-Barrier-Detector Diode Fabrication Using an Implanted Active Layer on High-Resistivity Silicon Substrate

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***Abstract*—A surface-oriented planar Schottky diode for use as a detector diode on Si monolithic microwave integrated circuits (MMIC's) was developed. The active n-on-n^+ and contact n^+ regions were doped on the high-resistivity silicon substrate using phosphorus ion implantation. The PtSi–Si barrier was formed by metallurgical interaction between pure platinum film and silicon. The process technology developed for the Schottky-detector diode fabrication is precise, simple, and cheap, and is suitable for mass production. The typical measured cutoff frequency of a zero-biased fabricated Schottky diode is 118 GHz.**

I. Introduction

THE USE OF high-resistivity silicon as the substrate material for monolithic microwave integrated circuits (MMIC's) has been discussed since 1965 [1]. Presently, circuits made on high-resistivity silicon substrates have been operated at frequencies above 40 GHz [2], and the price of commercial float-zone silicon wafers has dropped considerably [3]. For the fabrication of Si-MMIC's with integrated Schottky diodes, an active n-silicon layer on a localized area of the high-resistivity substrate is needed for the fabrication of the diodes. Further, a highly conductive n^+-silicon layer should be placed underneath the active n-silicon layer to minimize the series resistance of the diode. The thickness and doping profile of the active n-silicon layer with the buried n^+-silicon layer is very critical for the optimum characteristics of the microwave Schottky-barrier-detector diodes to be realized. The process for producing the active n-on-n^+ layer on the high-resistivity silicon substrate is the most important process step for the microwave Schottky diode fabrication. Several kinds of processes have been considered for this active layer formation. Up to now, molecular beam epitaxy (MBE) has frequently been the fabrication process used for the n-on-n^+ active-layer formation on the high-resistivity silicon substrate. MBE offers precise control of doping profile and thickness with nm resolution, and the low growth temperature has no harmful influence on the resistivity of the high-resistivity silicon substrate, but it is expensive, and it is difficult to realize growth in the selective regions of a planar diode structure.

A novel fabrication technology for microwave Schottky-detector diodes using a single implanted active n-on-n^+ layer in selective regions of the high-resistivity silicon substrate has been developed and is the subject of this paper. It is a precise and cheap process, and is suitable for mass production. The implantation results in a finely controlled doping profile with doping peak buried below the silicon surface to give the lightly doped n-silicon surface layer. The doping depth is easy to control by implanting energy level. A second lower energy implant is used to provide a heavily doped surface layer at the silicon contact regions to minimize contact and series resistance. Using this novel implantation process, Schottky diodes have been successfully produced on high-resistivity substrate suitable for silicon MMIC's.

II. The Structure of the Schottky Diode

The structure of the microwave Schottky barrier diode is shown in plan and cross-sectional views in Fig. 1. It is a surface-oriented planar diode structure that adopts a rectangular junction. The ohmic contact on the n^+-silicon layer encircles the rectangular Schottky junction on three sides. Both terminals of the junction lie on the same surface of the silicon substrate and are easy to connect to coplanar waveguide or microstrip transmission-line interconnects without introducing impedance mismatches. This geometry has been shown to significantly reduce the series resistance of the diodes, and has a higher cutoff frequency in comparison with a circular-junction structure due to extension of the length of junction periphery [4]. The substrates are 10-k$\Omega \cdot$ cm p-type $\langle 100 \rangle$ silicon wafers. The Schottky junction is formed on an n-on-n^+ region buried in the surface of the high-resistivity silicon substrate. The n-on-n^+ region is obtained with a single implant whose peak concentration is buried beneath the silicon surface.

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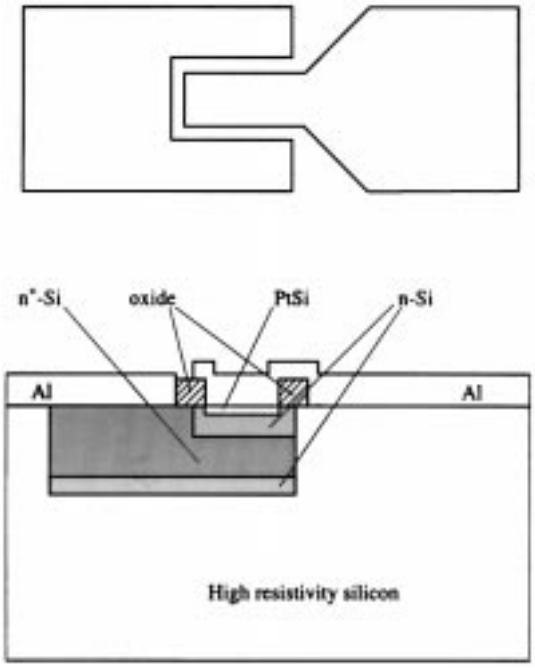


Fig. 1. The plan and cross-sectional view of the microwave Schottky diode.

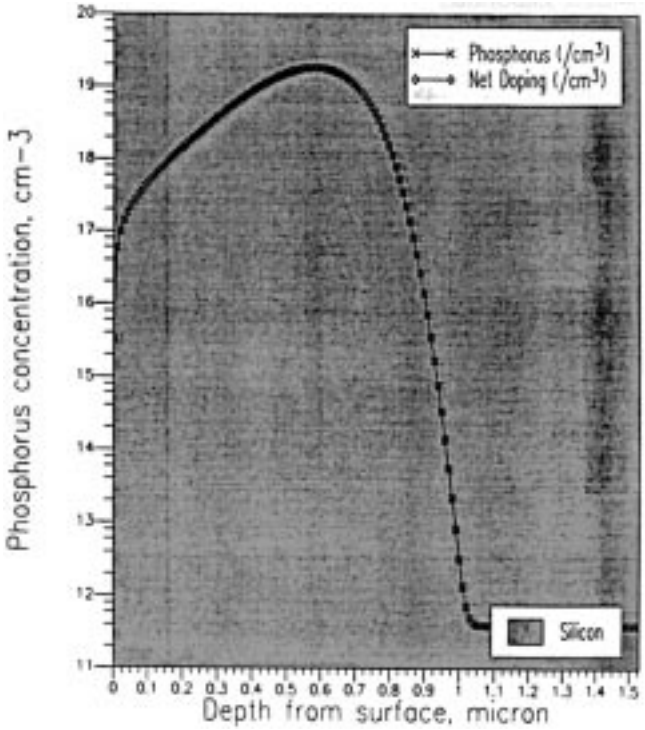


Fig. 2. The simulated optimum process for the active n-on-n^+ region implantation. 360-keV 6-e 14-implantation 950-C 20-min 720-C 2-h annealing.

The metallizations are contacted to the Schottky-barrier metal and to the n^+-silicon region, respectively, and then connected to a coplanar waveguide (CPW). The metal layers comprising the CPW line are directly in contact with the high resistivity silicon substrate in order to reduce microwave losses. For microwave-detector applications up to 40 GHz, a diode cutoff frequency of at least 80 GHz is required. The total capacitance and series resistance of the diode here must not be higher than 0.1 pF and 20 Ω, respectively; using a calculated Schottky junction area of 27 μm^2, and optimum doping concentration and thickness of n-silicon active layer of (1 $\sim$3) $\times$ 10^{17} cm^{-3} and (0.1$\sim$0.2) μm, respectively. The doping concentration of the buried n^+ layer must be higher than 1 $\times$ 10^{18} cm^{-3}. These values yield $R_S = 11\,\Omega$ and $C_T = 0.09$ pF using the procedures suggested for the design calculation for Schottky diodes as given in [5] and [6].

III. Implanted Active-Layer Formation and Schottky-Diodes Fabrication

According to the design calculations, for good microwave performance of Schottky detector diodes the implanted doping profiles of the active n-Si and contact n^+-Si layers should satisfy the following requirements.

1) The doping concentration at 500 Å underneath the wafer surface in the active n-on-n^+ silicon region is (1 $\sim$ 3) $\times$ 10^{17} cm^{-3} in order to get good I–V characteristics for the Schottky junction.
2) The layer thickness in the active n-on-n^+ silicon layer, where the donor concentration is higher than 1 $\times$ 10^{18} cm^{-3}, should not be thinner than 0.6 μm and the peak doping concentration should not be less than 1 $\times$ 10^{19} cm^{-3} in order to reduce the series resistance of the diode.
3) The doping concentration at the wafer surface in the contact n^+-Si region should not less than 1 $\times$ 10^{19} cm^{-3} to give low ohmic contact resistance with the contact metal.
4) The thickness of the n^+-Si layer, where the donor concentration is higher than 1 $\times$ 10^{18} cm^{-3}, should not be thinner than 0.8 μm in order to provide low diode series resistance.
5) The temperature of activation annealing should be lower than 1100 °C, to avoid changing the high-resistivity properties of the silicon substrate [7]. This ensures low losses of microwave circuits on the high-resistivity silicon substrate.

For the higher implanting energy, the series resistance of the diode should be lower due to the thicker active n-on-n^+. Using a standard 300-keV implanter, a 360 keV implanting energy was realized by using a 180-kV double-charge phosphorus ion implanting. A series of process simulations were performed to optimize the implantation process conditions for active n-on-n^+ silicon layer and contact n^+-silicon layer formation using the SSUPREM3 simulator. The optimum results of simulation are shown in Figs. 2 and 3. These are a 360 kV 6 $\times$ 10^{14} cm^{-2} phosphorus implant for the active n-on-n^+ layer, and a 360-kV 6 $\times$ 10^{14} cm^{-2} plus a 180-kV 2 $\times$ 10^{16} cm^{-2} phosphorus implant for contact n^+-Si layer formation. PtSi was selected as the Schottky-barrier metal. Formation of platinum silicide by metallurgical interaction between pure platinum film and silicon leads to the most reliable and reproducible Schottky barrier. The sintering temperature used to form the PtSi was in the range of 600 °C to 650 °C. When forming silicide by a platinum–silicon interaction, the

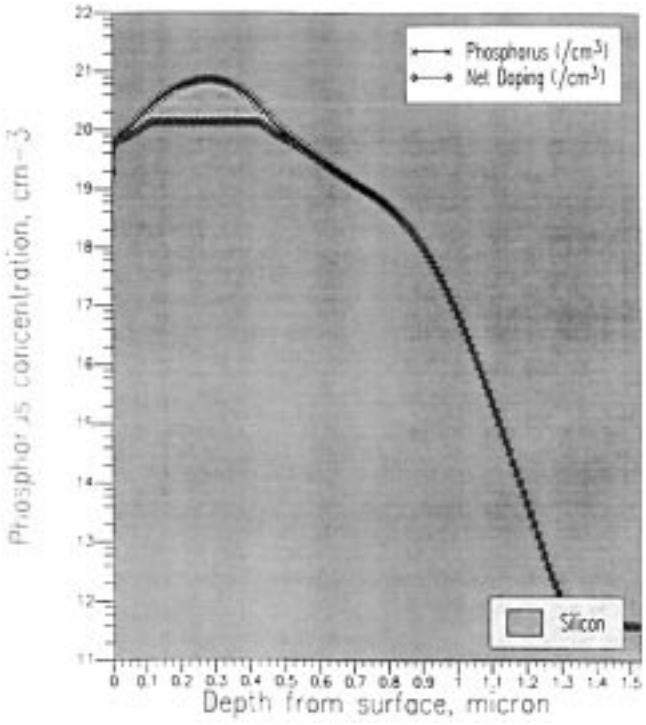


Fig. 3. The simulated optimum process for the contact n^+ region implantation. 360-keV 6-e 14-cm $-$ 2, and 180 keV 2-e 16-cm $-$ 2 implc 950-C 20-min and 720-C 2-h annealing.

amount of silicon consumed by the platinum film must be carefully considered because the requirement of junction depth is critical for optimum characteristics of Schottky detector diodes. This is due to the steep doping profile of the n-layer. The consumed silicon thickness if 1.32 times the thickness of platinum, and the thickness of the resulting platinum silicide is 1.98 times the thickness of platinum. A 400-Å thickness of platinum, to be deposited by electron beam (EB) gun evaporation, was selected for PtSi formation. Aluminum was used as contact metal for the diode and conductor metal for CPW interconnect due to its good process and electrical performance at microwave frequencies. It has been confirmed that the average RF conductivity for the aluminum is 2.3 $\times$ 10^7 S/m over the frequency range 1–40 GHz, and 1-μm-thick aluminum layer can usefully be employed as CPW interconnect metallization on high-resistivity silicon substrate [8].

The main flow of the fabrication process for the microwave Schottky diode on the implanted active region is shown in Fig. 4. The active n-on-n^+ layer is implanted using a deposited oxide tetraethyl orthosilicate (TEOS) mask and a 360-KV phosphorus ion implanting on the selective regions of high-resistivity silicon substrate. Secondly, a 180-KV phosphorus ion implanting forms the contact n^+ regions. The junction areas are opened on the final deposited oxide layer. The 950 °C 10 min N_2 annealing is used for densification of each deposited TEOS layer and also for activation of implanted layer. After the platinum EB evaporation and the 650 °C PtSi formation anneal, the unreacted platinum film on the oxide layer is selectively etched off using hot *aqua regia*. The PtSi is left on the junction areas. Lastly, the contact metallizations of

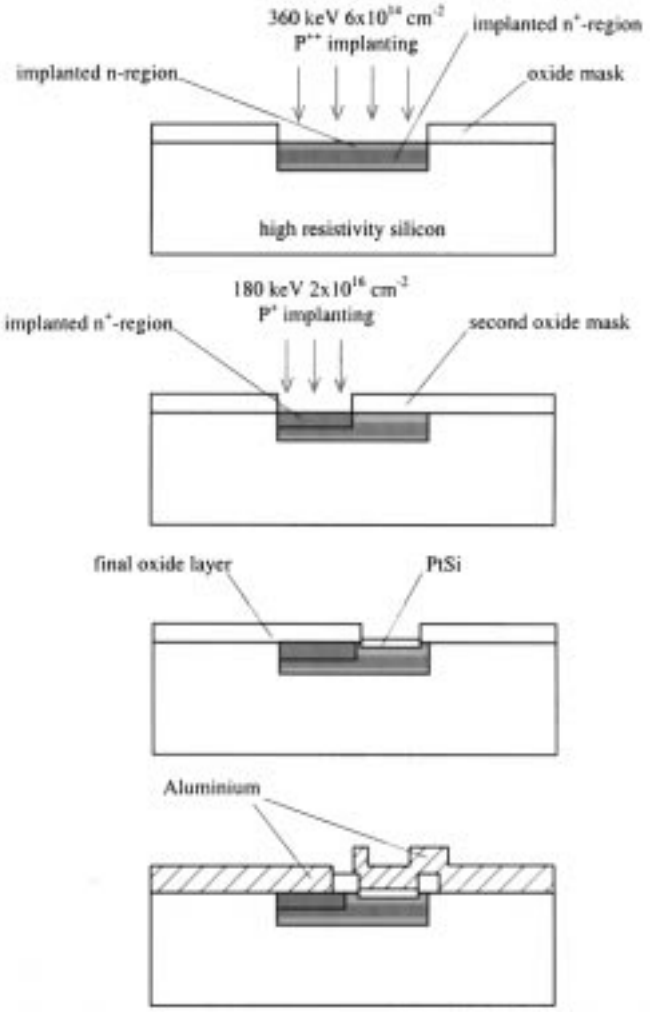


Fig. 4. The main flow of he fabrication process for microwave Schottky-detector diodes with implanted active region.

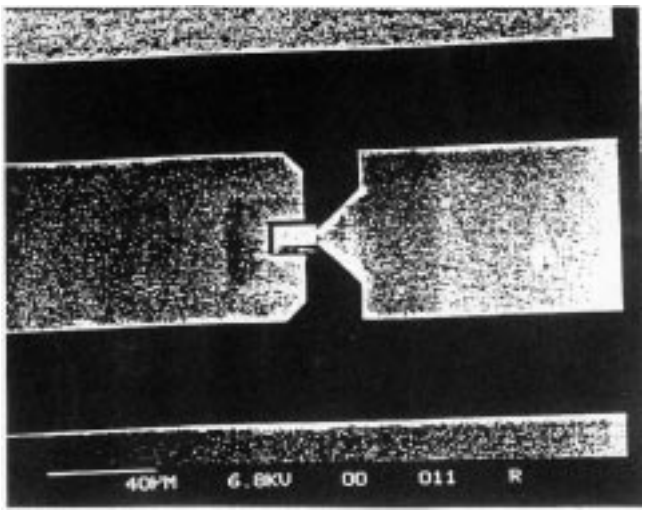


Fig. 5. Schottky-detector diode connected with CPW.

diodes and conductors of CPW's are deposited and patterned simultaneously. On the CPW line, the width of the signal trace is 70 μm and the signal-to-ground spacings are 40 μm, giving 50-Ω characteristic impedance on a 635-μm-thick high-resistivity silicon wafer.

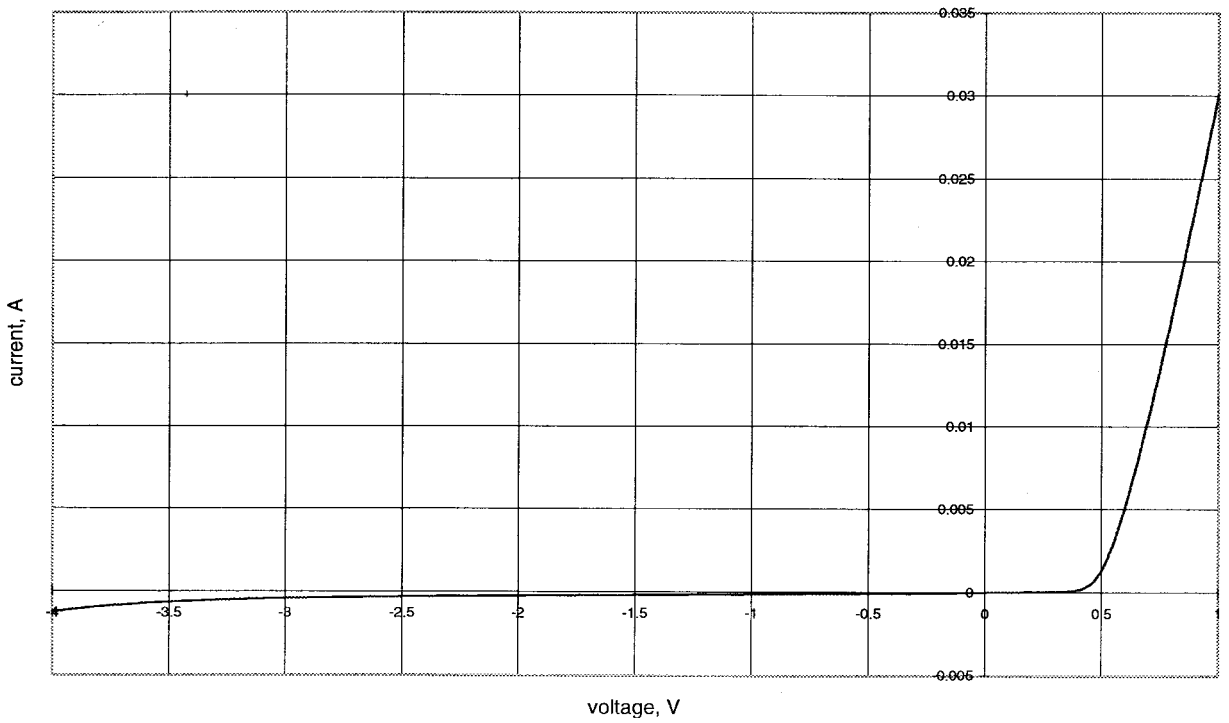


Fig. 6. Typical measured I–V characteristic of Schottky-detector diode.

TABLE I

ideality factor n	series resistance R_s at +10 mA, Ωe	forward voltage V_F at +1 mA, V	total capacitance C_r at 0 V, pF	reverse breakdown voltage V_B, V	saturation current I_0 A
1.40	11	0.48	0.09	4	6×10^{-10}

IV. Measurements and Discussion

An SEM microphotograph of the fabricated Schottky diode connected with CPW's is shown in Fig. 5. Figs. 6 and 7 are the measured typical I–V characteristics and the forward I–V characteristics, respectively. The measured typical dc parameters are listed in Table I. The dc test results show that the I–V and barrier characteristics of fabricated diodes are very good. These results confirm that implanted active regions on high-resistivity silicon substrates are suitable for the fabrication of Schottky-detector diodes.

From Fig. 7, an abnormal leakage current can be seen in the low forward-voltage region (<0.3 V). It has been found that the small leakage conductance $(G_{(V)})$ of the high-resistivity silicon substrate connected in parallel with the Schottky junction contributes the abnormal leakage current in the low forward-voltage region. The measured forward I–V characteristics of the diode is composed of the I–V characteristic of the Schottky junction and the leakage of the high-resistivity silicon substrate

$$I_{(V)} = I_0[\exp(\mathrm{qV/nkT}) - 1] + \mathrm{VG_{(V)}}.$$

The I–V characteristic of the Schottky junction has been determined by subtraction of the independently measured parallel leakage current, and the I_0 and ideality factor were subsequently determined on the normal way. The parallel leakage conductance $G_{(V)}$ can also be divided into two parts: the leakage conductance G_{cpw} between the center line and ground plate of the CPW, and the leakage conductance G_{na} between the n^+ region and anode metal interconnect of the diode due to the metal interconnects being directly in contact with the high-resistivity silicon substrate, as show in Fig. 8. This parallel leakage current is independent of the method of diode fabrication, and may be eliminated using a thin insulated layer between the CPW lines and the substrate.

For the forward biased detection, the bias voltage is higher than 0.4 V. Thus, the leakage of high-resistivity silicon substrate should only have a small effect on the operation of the detector. It has been confirmed that the measured line loss for biased CPW's with 1-μm-thick aluminum metallization on the high-resistivity silicon substrate is less than 1.5 dB/cm at 40 GHz [9].

The scattering parameters for the Schottky detector diodes, shunt mounted in a coplanar waveguide line, were measured in the frequency region of 2–40 GHz, Fig. 9 shows the equivalent circuit model for the diode. The diode parameters where modeled at a variety of bias voltages, and a multibias model extracted. The effect of two identical diodes shunt mounted, as shown in Fig. 10, has been taken into account in the diode model in Fig. 9. Table II shows the model parameters obtained at different bias voltages and the cutoff frequency for the diode calculated as

$$f_c = 1/(2\pi R_S C_J).$$

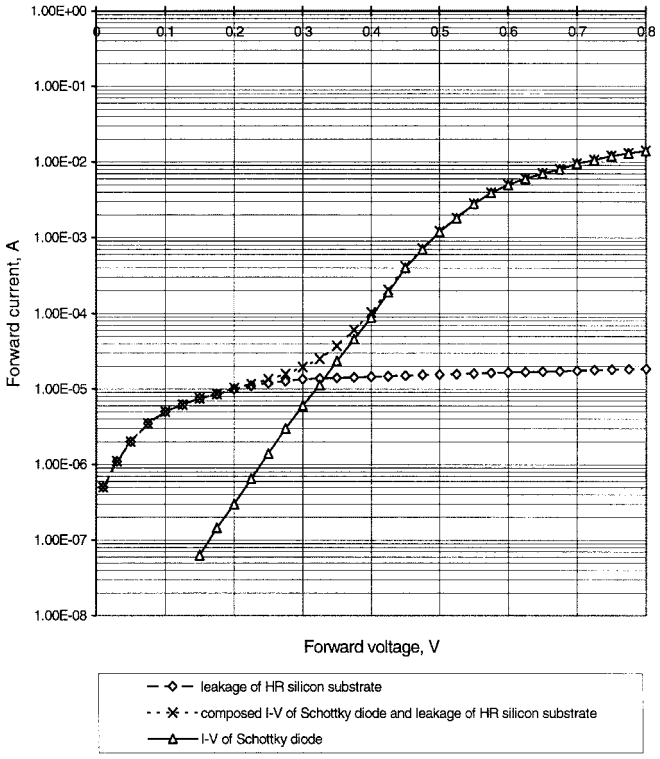
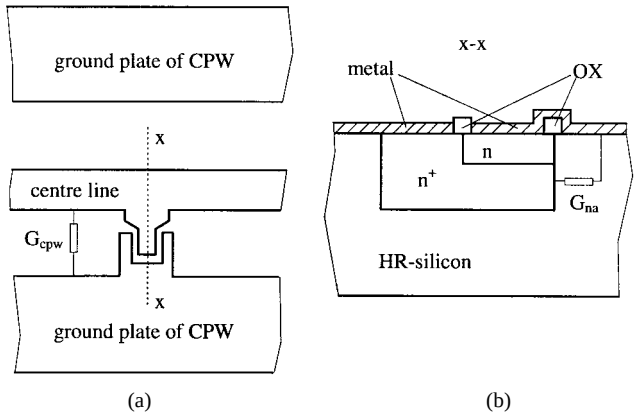


Fig. 7. Typical forward I–V characteristics of Schottky-detector diode connected with CPW on high-resistivity silicon substrate.



(a) (b)

Fig. 8. Leakage conductances of silicon substrate.

Here the ground–signal–ground (G-S-G) probed device measurements have been deembedded to the Schottky-diode pair x–x', as shown in Fig. 9. The cutoff frequency of the zero-biased Schottky-detector diodes determined using an equivalent circuit derived from S-parameters is approximately 118 GHz. Using the model values given in Table II, an MDS-based simulation predicts a value of current sensitivity of 1.17 μA/μW at 5 GHz and a bias of 0.5 V.

V. Conclusions

A fabrication technology for microwave-detector Schottky diodes using implanted active layer on the high-resistivity silicon substrate has been developed. It is a precise and cheap process, and is suitable for mass production. The new technology allows the simultaneous realization of microwave planar Schottky-detector diodes and CPW interconnect lines on the same surface of the high-resistivity silicon substrate. There is an observable leakage current in the low forward-voltage region of the I–V characteristic of the Schottky diodes due to the inherent leakage of the CPW lines on high-resistivity silicon substrate, but it should only have a small effect on the operation of the detector when operate with forward bias. The parallel leakage path can be eliminated by including an insulating layer between the CPW and the substrate. The fabricated Schottky diode shows dc and microwave performance

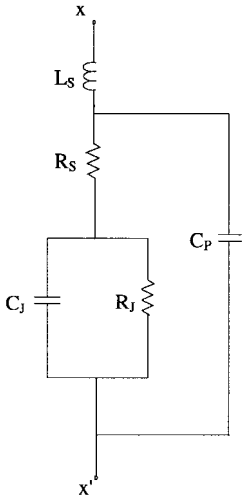


Fig. 9. Equivalent-circuit model for the Schottky diode.

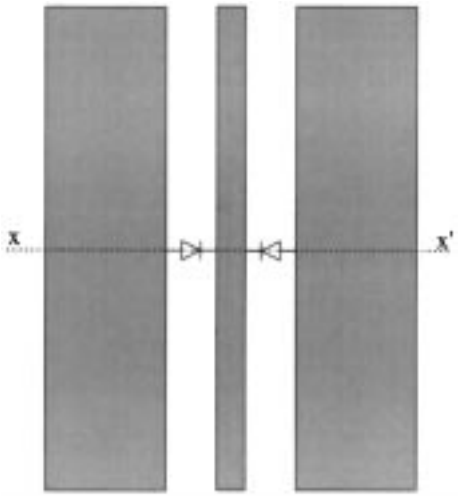


Fig. 10. Two diodes symmetrically connected across a CPW line.

TABLE II

biased voltage V	L_S pH	R_S Ω	C_J pF	R_J Ω	C_P pF
-2.2	31.7	22.9	0.0554	8.80×10^5	0.0304
-1.4	27.8	19.5	0.0677	8.80×10^5	0.0299
-0.6	26.5	18.7	0.0822	6.10×10^5	0.0354
0.0	26.5	12.9	0.104	5.20×10^5	0.0487
0.8	34.3	10.68	0.199	0.63	0.133

comparable with that of epitaxially grown devices. The typical measured cutoff frequency of a zero-biased fabricated detector Schottky diode is 118 GHz.

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Harold S. Gamble (M'95), for photograph and biography, see this issue, p. 631.

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